METHOD FOR MANUFACTURING A SEMICONDUCTOR DEVICE

FIELD OF THE INVENTION

The present invention relates to a method for manufacturing a semiconductor device, and particularly to a method for manufacturing a semiconductor device including a step of forming a conductive path extending from an insulating layer on a semiconductor substrate to a conductive member embedded in the insulating layer.

RELATED ART

To form a conductive path extending from an insulating layer on a semiconductor substrate to a conductive member embedded in the insulating layer, JP-A-11-233632 discloses a method by which to form a through-hole in the insulating layer which leads to the conductive member, and then fill the through-hole with a conductive material.

In the method disclosed in the above publication, when the through-hole is displaced from where it is aligned with the conductive member, if, by this misalignment, the unaligned recess portion of the through-hole, which extends downwardly from the conductive member, reaches a lower conductive member located beneath or any conductive part on the substrate, a short-circuit problem arises. As a measure to prevent this short-circuit, to stuff up the unaligned recess portion with an insulating material, a new insulating film is deposited on the whole of the insulating layer, including the internal wall of the through-hole. After this new insulating layer has been deposited, the unnecessary portion of the deposited insulating layer is removed by etching, and then the through-hole, whose unaligned recess portion has been stuffed up, is filled with a conductive member, by which the conductive path leading to the

conductive member is formed without causing a problem such as a short-circuit of the conductive path caused by misalignment.

However, according to the prior art mentioned above, as described above, it is necessary to perform a step of stuffing with a new insulating material the unaligned recess portion extending downwardly from the conductive member caused by misalignment of the through-hole and an etching step to remove the unnecessary portion of the deposited insulating layer, and by these steps, the manufacturing process of a semiconductor device is complicated, and it is not easy to appropriately control the thickness of the deposited insulating material used to stuff the unaligned recess portion.

Because the unaligned recess portion of the through-hole is stuffed with an insulating material, the effective bore diameter of the through-hole is reduced if a filling material is deposited with an immoderate thickness, and the electrical resistance of the conductive path used to fill the through-hole is increased.

Therefore, the object of the present invention is to provide a method for manufacturing a semiconductor device including a conductive path by which to fill the through-hole, and a method for manufacturing a semiconductor device relatively easily which can prevent an increase in the electrical resistance of the conductive path that fills up the through-hole without making the manufacturing process more complicated or causing the short-circuit problem resulting from misalignment of the through-hole.

SUMMARY OF THE INVENTION

The inventor of the present invention makes a finding that when a reactive ion etching unit is used to form an etched hole for a conductive path extending from the insulating layer of silicon dioxide on a semiconductor

substrate to the conductive member embedded in the insulating layer and a mixed reaction gas consisting of CHF_3/CO is supplied to the reaction chamber by feeding the respective component gases at specified flow rates, etching takes place but comes to a stop without progressing to such an extend as causing the short-circuit problem as in the past so long as misalignment of an etching mask is within a permissible error.

The present invention utilizes this etching stop phenomenon. According to an aspect of the present invention, there is provided a method for manufacturing a semiconductor device having a conductive path extending from an upper surface of an insulating layer of silicon dioxide on a semiconductor substrate to a conductive member embedded in the insulating layer, comprising the steps of forming on the insulating film an etching mask defining an etched hole for the conductive path within a permissible placement error, performing a selective etching process to the insulating layer to remove a region of the insulating layer not covered by the etching mask by using a reactive ion etching unit for introducing into a reaction chamber reactive gas of CHF_3/CO components, respectively flowing at a flow ratio of about 15/85, and filling the hole formed by the etching process with a conductive material for the conductive path.

It has been clarified that according to the present invention, when the pressure of the reaction chamber of the reactive ion etching unit is not less than 100mTorr and the high-frequency power of the etching unit is 1600W, if the placement error, or the misalignment, of the etching mask is not more than 0.04μm, the etched hole is not formed deeper than 300nm from the surface of the conductive member.

The etching stop phenomenon that the progress of etching stops before the depth of the conductive member reaches 300nm means that the etched hole

is shallow enough not to reach the lower conductive member located under the conductive member or the semiconductor substrate. In other words, when the flow rates of CHF_3 and CO are set at about 30sccm and about 170sccm, for example, by placing the etching mask within a permissible placement error of 0.04μm, it is possible to prevent the etched hole from reaching a region where a problem could arise, such as a short-circuit, caused by misalignment of the etching mask.

Therefore, the unaligned portion of the etched hole due to misalignment of the etching mask need not be stuffed with an insulating material as in the past, and by merely filling the etched hole with a conductive material, the conductive path leading to the conductive member in the insulating layer can be formed without causing a short-circuit.

With an intention of ensuring that the pressure of the reaction chamber of the reactive ion etching unit was not less than 200mTorr and the flow rate of a reactive gas was not less than about 300sccm, when the flow rates of CHF_3 and CO were set, for example, at about 45sccm and about 255sccm, the etching stop phenomenon was witnessed in which the etched hole did not advance deeper than about 100nm from the surface of the conductive member so long as the placement error of the etching mask was less than 0.1μm.

Therefore, by setting the pressure of the reaction chamber of the reactive ion etching unit at 200mTorr or higher and the flow rate of a reactive gas at about 300sccm or higher, a short-circuit can be prevented more securely and a larger permissible placement error can be assigned to the etching mask.

According to another aspect of the present invention, another method for manufacturing a semiconductor device having a conductive path extending from an upper surface of an insulating layer of silicon dioxide on a semiconductor substrate to a conductive member embedded in the insulating

layer, comprising the steps of forming on the upper surface of the insulating layer an etching mask defining an etched hole for the conductive path extending to the conductive member within a permissible placement error, performing a selective etching process to the insulating layer by using a reactive gas to remove a region of the insulating layer not covered by the etching mask, depositing a polymeric product by a polymeric film generating action of the reactive gas into an etched groove resulting from the misalignment of the etching mask, and filling the etched hole formed by the etching process with a conductive material for the conductive path.

As the above-mentioned reactive gas, a mixed gas of CHF_3 and CO may be used. The flow rate of the mixed gas is preferably about 300sccm or higher and the reactive gas pressure in the reaction chamber is preferably 200mTorr or higher.

BRIEF DESCRIPTION OF THE DRAWINGS

Figs. 1(a)~1(d) are sectional views schematically showing the steps of a manufacturing method of a semiconductor device according to the present invention;

Fig. 2 is a sectional view schematically showing a reactive ion etching unit for carrying out a manufacturing method according to the present invention shown in Fig. 1;

Fig. 3 is a graph (1) showing the etching characteristics of the insulating layer when the reaction chamber pressure was varied by mixed-gas fixed flow rates in the reactive ion etching unit according to the present invention; and

Fig. 4 is a graph (2) showing the etching characteristics of the insulating layer when the reaction chamber pressure was varied by mixed-gas

fixed flow rates in the reactive ion etching unit according to the present invention.

DESCRIPTION OF A PREFERRED EMBODIMENT

The present invention will be described in detail with reference to an embodiment illustrated in the accompanying drawings.

Figs. 1(a)~1(d) show steps of a method for manufacturing a semiconductor device according to the present invention.

Referring to Fig. 2, description will first be made of an example of a reactive ion etching unit used for carrying out the present invention before moving to the description of a manufacturing method according to the present invention with reference to Figs. 1(a)~1(d).

A reactive ion etching unit 10 according to the present invention is a dipole ring magnetron reactive ion etching (RIE) unit in the example shown in Fig. 2. As has been well known, the dipole ring magnetron reactive ion etching unit 10 includes a plurality of permanent magnets 13 arranged surrounding a housing 12 which defines the reaction chamber 11.

An etching gas is supplied from a supply port 14 to the reaction chamber 11 through gas blowout holes 16 of an upper electrode 15. The etching gas is discharged from the reaction chamber 11 through an exhaust port 17, formed in the housing 12, which is connected to an exhauster, not shown.

The upper electrode 15 is grounded together with the housing 12 to keep the etching gas supplied to the reaction chamber 11 in plasma state, and to a sample holder 19 serving as the lower electrode on which a processing sample 18 is mounted, as is well known, high-frequency power is supplied from a high-frequency power source 21 through a blocking capacitor 20 to block a

DC component of voltage.

The permanent magnets 13, as is well known, are driven to rotate around the housing 12 so that their magnetic forces can increase the plasma density in the reaction chamber 11 to thereby improve the etching effect by etching gas.

According to the etching method according to the present invention, as the etching gas supplied to the reaction chamber 11, a mixed gas of CHF_3 and CO is used.

An example of a semiconductor device which is subjected to an etching process by the above-mentioned mixed etching gas is shown in Figs. 1(a)~1(d).

As shown in Fig. 1(a), a semiconductor device 18 arranged as a sample on the sample holder 19 includes a semiconductor substrate 22, such as silicon, and an electrode member 24 made of a metal material, such as aluminum, embedded as a conductive member in an insulating layer 23 made of silicon dioxide formed on the semiconductor substrate.

In the example shown in Fig. 1(a), in the insulating layer 23, a second conductive member is embedded as a lower electrode member below the electrode member 24.

For simplicity of drawing, the semiconductor substrate 22 is omitted in Figs. 1(b)~1(d).

The reactive ion etching unit 10 is used to form an etched hole for a conductive path extending from the surface 23a of the insulating layer 23 down to the electrode member 24. Before the etching process by the reactive ion etching unit 10, as shown in Fig. 1(b), as is well known, a resist mask 26 made of a photoresist material is formed on the surface 23a by photolithography.

In the resist mask 26, an opening 26a is formed with a diameter D1 of 0.2~0.3m, for example, which substantially corresponds to the width of the

electrode member 24. The reactive ion etching unit 10 is used to remove a region of the insulating layer 23 exposed through the opening 26a to thereby form an etched hole 27 leading to the electrode member 24. For a selective etching process to form the etched hole 27, the semiconductor device is placed on the sample holder 19 such that the surface 23a of the insulating layer 23 faces the upper electrode 15 of the reactive ion etching unit 10.

In the present invention, as a mixed gas introduced into the reaction chamber 11 from the supply port 14 of the reactive ion etching unit 10, a mixed gas of CHF_3 and CO is used as mentioned above.

By using a mixed gas of CHF_3 and CO is used as an etching gas, the region of the insulating layer 23 exposed through the opening 26a of the resist mask 26 is selectively removed by etching. Therefore, when the opening 26a of the resist mask 26 is formed at a position where the opening 26a is aligned with the electrode member 24, an offset of the opening 26a with respect to the electrode member 24 as shown in Fig. 1(b) does not occur. Consequently, when the etched hole extends right onto the electrode member 24, the electrode member 24 serves as an etching stopper, so that the etched hole is formed to open in correct alignment with the electrode member 24.

In contrast, if the semiconductor device 18 receives an etching process under the condition that there is an offset g caused by misalignment of the resist mask 26, the offset g of the etched hole 27 is likely to extend below the electrode member 24 and reach the lower electrode member 25.

The inventor discovered the etching stop condition by which to prevent the etched hole from reaching the lower electrode member 25 even if an offset of the opening 26a is caused by misalignment of the resist mask 26 in the etching process in the reactive ion etching unit 10 where the mixed gas is introduced into the reaction chamber 11.

Because the reaction by an etching gas generally includes an etching action and a polymerizing action, in the above-mentioned etching process, in addition to an etching action, a polymerizing action takes place which deposits a polymeric product on the etched portion. Under the above-mentioned etching stop condition, a polymeric product produced by the polymeric film generating action by the etching gas is deposited in the etched groove (s), which is formed to correspond to an offset s caused by misalignment of the resist mask 26, and as the etching action and the polymerizing action are balanced, it appears that the etching stop phenomenon manifests itself.

Fig. 3 is a graph (1) obtained from results of an experiment to find the etching stop condition, in which the horizontal axis denotes offsets s (in μm) of the resist mask 26 and the vertical axis denotes depths d (in μm) (see Fig. 1(c)) of the unaligned recess portion of the etched hole 27 from the upper surface of the electrode member 24 by etching for one minute.

This experiment was conducted while CHF_3 and CO were supplied to the reaction chamber 11 respectively at flow rates of about 30sccm and about 170sccm so that the flow ratio of CHF_3 and CO was about 15/85 and output of the high-frequency power source 21 was maintained at 1600W. The relation between the depth d and the offset s of the resist mask 26 was obtained after the etching process was carried out for one minute with the pressure of the reaction chamber 11 varied as a parameter.

In the graph (1) of Fig. 3, the characteristic curves 28, 29, 30 and 31 show relations between the depth d and the offset s at reaction chamber pressures of 200mTorr, 100mTorr, 75mTorr and 50mTorr.

The etching stop phenomenon was not observed during a one-minute etching process at a point indicated by a code 28a on the characteristic curve 28 and at a point indicated by a code 29a on the characteristic curve 29, but the

etching stop phenomenon did not take place at any other points on the other characteristic curve.

More specifically, under the condition that the pressure in the reaction chamber 11 was 100mTorr, when the offset of the resist mask 26, or a placement error, was 0.04μm, the etching stop phenomenon was observed at a depth of about 250nm from the upper surface of the electrode member 24.

Under the condition that the pressure in the reaction chamber 11 was 200mTorr, when an error in placing the resist mask 26 was 0.05μm, the etching stop phenomenon occurred at a depth of about 150nm from the upper surface of the electrode member 24.

From the tendency shown in the graph (1) of Fig. 3, as the pressure of the reaction chamber 11 is increased, the placement error at which the etching stop phenomenon occurs is considered to increase. Therefore, it is understood that the depth d (in nm) of the unaligned portion of the etched hole 27 from the upper surface of the electrode member 24 does not exceed 200nm when the pressure of the reaction chamber 11 is maintained at 100mTorr or higher so long as the error in placing the resist mask 26 is not more than 0.04μm.

Referring back to Fig. 2(c), a distance H from the upper surface of the electrode member 24 to the lower electrode member 25 is generally larger than 300nm.

Therefore, if the permissible placement error of the resist mask 26 is limited to 0.04μm and the resist mask 26 is placed properly within this error limit, by performing the etching process to the insulating layer 23 under the condition that the reaction chamber pressure is maintained at 100mTorr or higher while supplying the reaction chamber 11 of the reactive ion etching unit 10 with a mixed reaction gas of CHF_3 and CO at a flow ratio of about 15/85 for these component gases, as shown in Fig. 2(c), the unaligned portion due to the

offset s of the etched hole 27 never reaches the lower electrode member 25 even if there is an offset within the permissible error.

Therefore, when the placement error of the resist mask 26 is not more than 0.04μm, without stuffing up the unaligned portion due to the offset s of the etched hole 27 by an insulating material as in the prior art, the conductive path 32a, which extends from the upper surface 23a of the insulating layer 23 to the electrode member 24, can be formed relatively easily by merely removing the resist mask 26 and then filling the etched hole 27 including the unaligned portion with a conductive material 32 as shown in Fig. 1(d), with no possibility of a short-circuit occurring in the lower electrode member 25.

According to the above-mentioned method of the present invention, as described above, there is no need to stuff up the unaligned portion of the etched hole 27 caused by an offset of the resist mask 26, and therefore the conductive path 32a that fills up the etched hole 27 is not reduced in diameter and an increase in electrical resistance, which would otherwise arise, can be prevented.

Ins A6

Fig. 4 is a graph (2) obtained from results of an experiment to find the etching stop condition, in which, as in the graph (1) of Fig. 3, the horizontal axis denotes offsets s (in μm) of the resist mask 26 and the vertical axis denotes depths d (in μm) (see Fig. 1(c)) of the unaligned portion of the etched hole 27 from the upper surface of the electrode member 24 by etching for one minute.

In the experiment to obtain the graph (2) in Fig. 4, the relation the depth d after one-minute etching and the offset s of the resist mask 26 when the mixed gas was supplied to the reaction chamber 11 at flow rates of CHF_3/CO of 10/57sccm, 30/170sccm, 36/204sccm and 45/255sccm so that the CHF_3/CO flow ratio of about 15/85 under the condition that the pressure of the reaction chamber 11 was maintained at 200mTorr and output of the high-

frequency power source 21 was maintained at 1600W.

The characteristic curves 33, 34 and 35 in the graph (2) of Fig. 4 show the relation between the depth d and the offset s of the resist mask 26 at flow rates of CHF_3/CO of 45/255sccm, 36/204sccm, 30/170sccm and 10/57sccm.

The etching stop phenomenon was observed in a one-minute etching process respectively at points indicated by codes 33a, 33b and 33c on the characteristic curve 33, at points indicated by codes 34a and 34b on the characteristic curve 34, and at a point indicated by a code 35a on the characteristic curve 35, but the etching stop phenomenon was not observed at any other points on the other characteristic curve.

As is clear from the graph (2) of Fig. 4, it is understood that the etching stop phenomenon is observed at a depth of about 100nm from the upper surface of the electrode member 24 under the condition that the pressure of the reaction chamber 11 is 200mTorr when the flow rates of CHF_3/CO of not less than 300sccm, such as 45/255sccm if the offset s of the resist mask 26 is not more than 0.1μm.

Therefore, by setting the pressure of the reaction chamber 11 in the reactive ion etching unit at 200mTorr or higher and the flow rate of the reactive gas at about 300sccm or higher, a short-circuit can be prevented more securely and a larger permissible placement error can be assigned to the etching mask.

In the foregoing, description has been made of an example in which the lower electrode member was disposed below the electrode member embedded in the insulating layer made of silicon dioxide; however, the present invention is not limited to this example, but can be effectively applied to a case where under the condition that a conductive part of a semiconductor substrate or some other conductive part is placed below the electrode member in the

some other conductive part is placed below the electrode member in the insulating layer including silicon dioxide, a short-circuit to such a conductive part as mentioned above is to be prevented and a conductive path is to be securely formed to extend to the above-mentioned electrode member without causing an increase in electrical resistance.

Instead of the above-mentioned dipole rink magnetron reactive ion etching unit, various types of reactive ion etching units can be used.

According to a method for manufacturing a semiconductor device of the present invention, as described above, by utilizing the etching stop phenomenon, it is possible to prevent an unnecessary extension of the etched hole caused by misalignment of the etching mask, which is responsible for the short-circuit problem, and therefore an appropriate conductive path can be formed without stuffing the unaligned portion of the etched hole resulting from the misalignment by an insulating material as in the prior art.

Consequently, it is possible to preclude various defects, which used to occur in the prior caused by stuffing the unaligned recess portion of the etched hole by an insulating material. For this reason, it becomes possible to produce a semiconductor device that can prevent an increase in electrical resistance of the conductive path that fills up the through-hole without increasing complexity of the manufacturing process or incurring the short-circuit problem.